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J Gateley, M Blatt, D Chen, S Cooke, P Desai, M ... - Proceedings of the Design Automation Conference (DAC), 1995 - portal.acm.org

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P Zadarnowski, U Thesis - BE thesis, School of Computer Science and Engineering, ..., 2000 - cse.unsw.edu.au ... Instruction set (ISA) **simulation** is an established technique used for debugging, profiling and validation of com- puter systems since the introduction of the ...

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IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language

IS Board - 1995 - ieeexplore.ieee.org

... and supported verification simula- tion, timing analysis, fault simulation, and test ... Miriam Blatt James Brandt Dennis B. Brophy Randal E. Bryant John A. Busco ... Web Search - larc.ee.nthu.edu.tw

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A Bogliolo, L Benini, G De Micheli, B Ricco - IEEE TRANS VERY LARGE SCALE INTEGR VLSI SYST, 1997 ieeexplore.ieee.org

... 2. Peak current versus overall power consumption of ... Data are obtained by electrical-level simulation. ... Gate Model When evaluating the average power consumption ... Cited by 17 - Web Search - chronos.stanford.edu - si2.epfl.ch - sti.uniurb.it - all 10 versions »

Clock skew optimization for peak current reduction

L Benini, P Vuillod, A Bogliolo, G De Micheli - Journal of VLSI Signal Processing, 1997 - springerlink.com ... approx- imation of the average current profile. ... to the combinational logic from simulation of our ... effective optimization algorithm for peak current minimization ... Cited by 10 - Web Search - kluweronline.com - ingentaconnect.com - portal.acm.org - all 6 versions »

Modelling utility-scale wind power plants. Part 1: Economics

MR Milligan - Wind Energy, 1999 - doi.wiley.com ... of the other units with probabilistic simulation algorithm ... This average cost can, at the modeller's option, include ... capacity on-peak for the o□-peak target to ... Cited by 7 - Web Search - nrel.gov - dlnet.vt.edu - adsabs.harvard.edu

Study of power consumption for high-performance reconfigurable computing architectures BF Veale, N Lopez-Benitez - 1999 - students.ou.edu

... This approach requires the simulation of time-domain data ... over the entire interval corresponding to the input data ... fourth clock cycle, on average, and a value ... Cited by 1 - View as HTML - Web Search - cs.ou.edu - cs.ou.edu

воом Logic synthesis for low power VLSI designs

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Initial results on the performance and cost of vector microprocessors

CG Lee, DJ DeVries - PROC ANNU INT SYMP MICROARCHITECTURE. pp. 171-182. 1997, 1997 - portal.acm.org

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Paul Gingras - Sun Microsystems, Inc.,. Burlington, MA. Scott Reedstrom - Guidant Corp.,

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